

Rev. Date Author Revision Description

R0A	Jan - 22 - 2015	Forbidian Kuo	R0A Release
R0B	Jan - 28 - 2015	Forbidian Kuo	1. Update mSATA symbol, reverse RX P/N 2. update B2B CONN footprint 3. change DDR4 VDDSPD to P3V3_A
R0B	06 - 01 - 2015	Forbidian Kuo	1. unpopulate R170 2. R454 change to 10k connect to P3V3 3. R291 change to 10k 4. R597/R232/R627/R274 change to 4.7k 5. R244 change to 10k 6. R259 unpopulated 7. R554 / R9 change to 1k 8. PCIE ac coupling change to 0.22uF 9. KR ac coupling change to 0.1uF
R0B	06 - 04 - 2015	Forbidian Kuo	1. Modify B2B CONN Pin assignment 2. Add CONN18 for external console board 3. modify JTAG train circuit 4. Add strap function table 5. Modify power for ripple (add cap)
R0B	07 - 13 - 2015	Forbidian Kuo	1. change conn2/conn17 footprint
R0B	07 - 13 - 2015	Forbidian Kuo	1. change U36 to PCA9617
R0C	10 - 03 - 2015	Forbidian Kuo	1. R279 change to 71.5k for P3V3_A HV issue 2. add R846/R847/C705/C706 for MIIM SI issue 3. SGMII_RX reverse issue 4. L11 change to same as L20 5. add C904/C907 for P3V3_A SI 6. CONN18 change to P2.54 ver
R0C	10 - 05 - 2015	Forbidian Kuo	1. change L40 to small one 2. reserve DDR_VPP power for R878/R877/R880 3. Add R881/R882 for MAC RESET 4. change BCM 3.3V from P3V3_A to P3V3_A_L_BCM 5. Add U7 for main board JTAG/SPI
R0C	10 - 14 - 2015	Forbidian Kuo	1. remove cpu CPLD from JTAG train, simple the JTAG topology
R0C	10 - 29 - 2015	Fajung_Liu	1. Modify HS1 footprint 2. H3-H6 change to NUT1-NUT6
R01	02 - 22 - 2016	Forbidian Kuo	1. Modify BDX_CPLD_JTAG_TCK_R / BDX_CPLD_JTAG_TDI_R / BDX_CPLD_JTAG_TD0_R net name 2. Change C255, C258, -C607, -C633 from 204000000353A to 2041033JE110J 3. P3V3_A change to be supplied from P5V_STBY 4. Mod UART0 topology for chassis purpose 5. Connect BDX GPIO1,6,7,17,68,69 to CPLD
R01	02 - 23 - 2016	Fajung_Liu	1. Remove SGMII TX side AC Coupling (P37) 2. Modify CLK_33M_LPC voltage level 1.1V to 1.05V (P16) 3. C51 and C52 CL 18pF change to 12pF (P16) 4. C103 and C105 CL 27pF change to 15pF (P14) 5. C649 27pF change to 22pF, C650 27pF change to 18pF(P35)
R01	03 - 03 - 2016	Forbidian Kuo	1. Change M.2 Nut hole to 2 npth oval hole 2. Remove GPIO6/7/69 from cpu to cpld
R02	04 - 26 - 2016	Fajung_Liu	1.Modify error net name (P29) 2.Modify error net name U17 pin 7(P17) 3.Add pull up resister to 3.3V (P37)
R02	06 - 27 - 2016	Fajung_Liu	1.Add BMC Function 2.Modify BMC remote SPI update
R0A	05 - 11 - 2018	Dino_Lin	1.To re-Layout CPU Board by project design request and to change version from R02 to R0A. 2.To change ethernet control from BCM5720 to Intel WGI210IT. 3.To change the part from commerce grade to industry grade. (BDX D-1518 to D-1519 & TPM chipset)

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08_Power Sequence
09_Strap Function
10_blank
11_RP_DDR4_SODIMM1
12_RP_DDR4_SODIMM2
13_RP_PCIE
14_BDX-DE_10GBEthernet
15_BDX-DE_SATA_USB
16_BDX-DE_Clock
17_BDX-DE_SYSTEM
18_BDX-DE_STRIP
19_BDX-DE_GND
20_BDX-DE_Power
21_BDX-DE_CPU_XDP_CONN
22_BDX-DE_PCH_XDP_CONN
23_CPLD_1
24_CPLD_PWR_P3V3_A_P1V8A
25_SMBUS Device
26_B2B Connector
27_Level Shifter
28_SPI
29_VCCIN_P1V05
30_P1V2_VDDQ_DDR4_VPP_P06_VTT
31_P3V3_P5V
32_1.3V_1.7V_P1V5_PCH

33_DEBUG_LED
34_BMM_CONN
35_WGI210IT Ethernet_CTRL

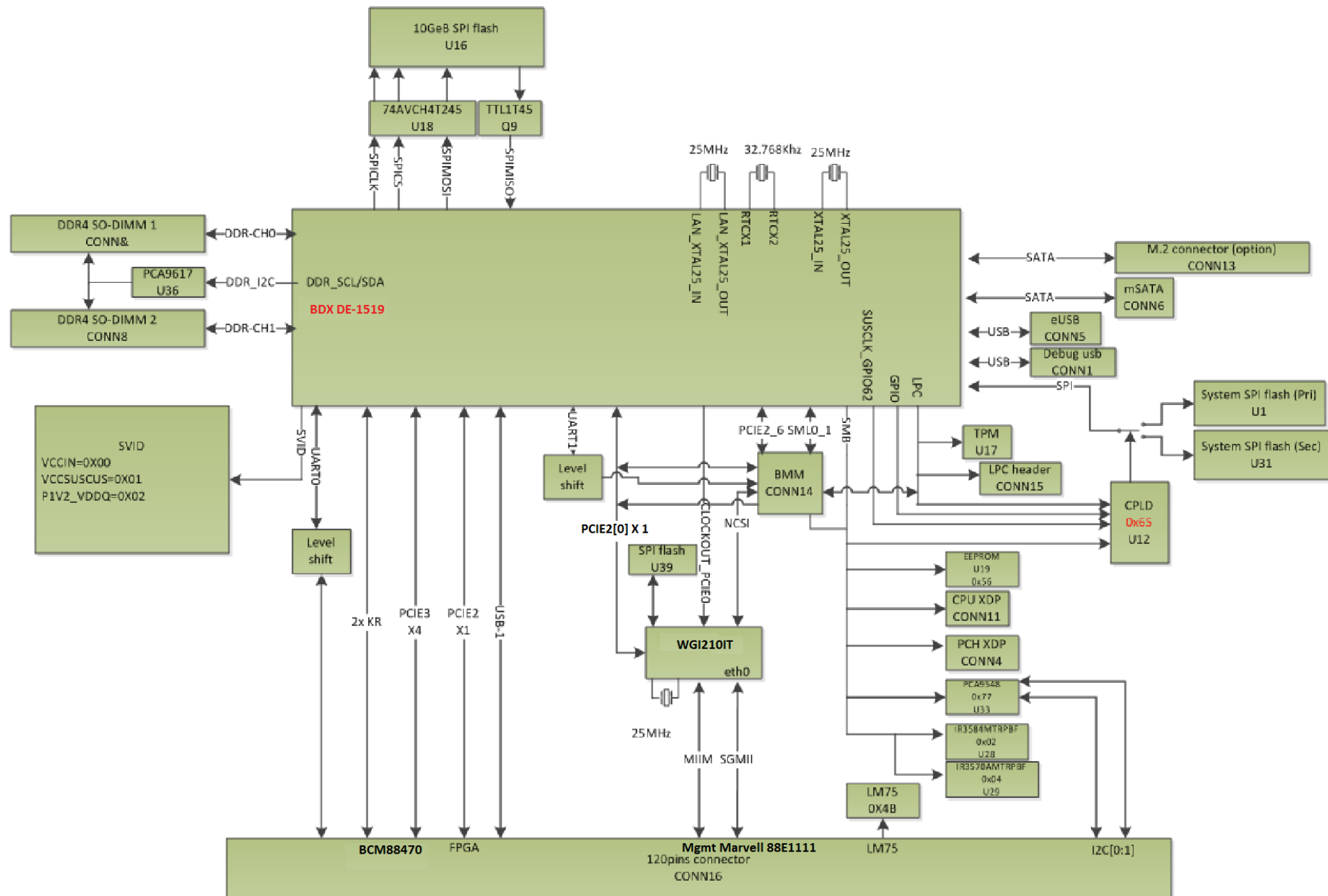
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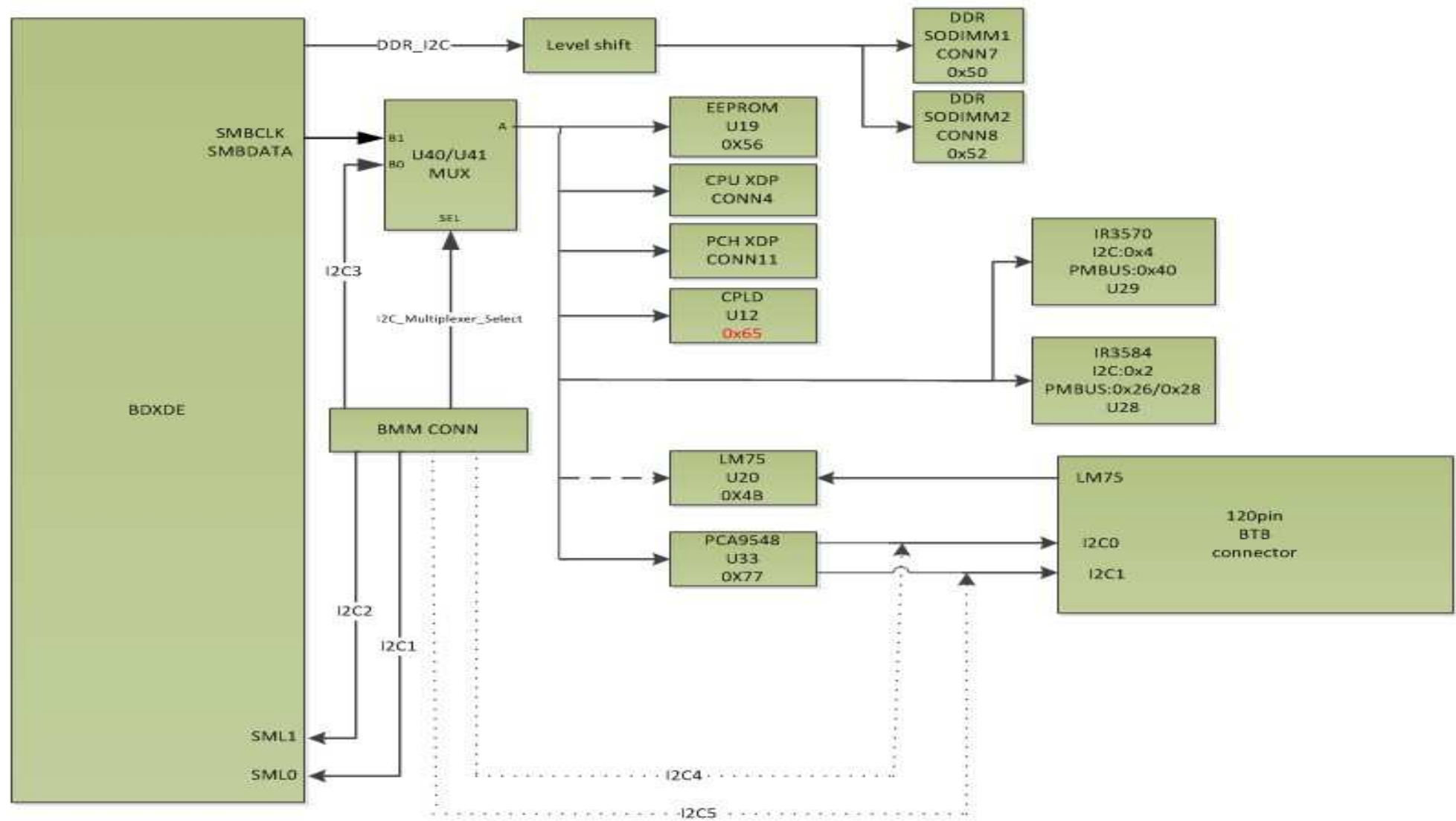
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Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

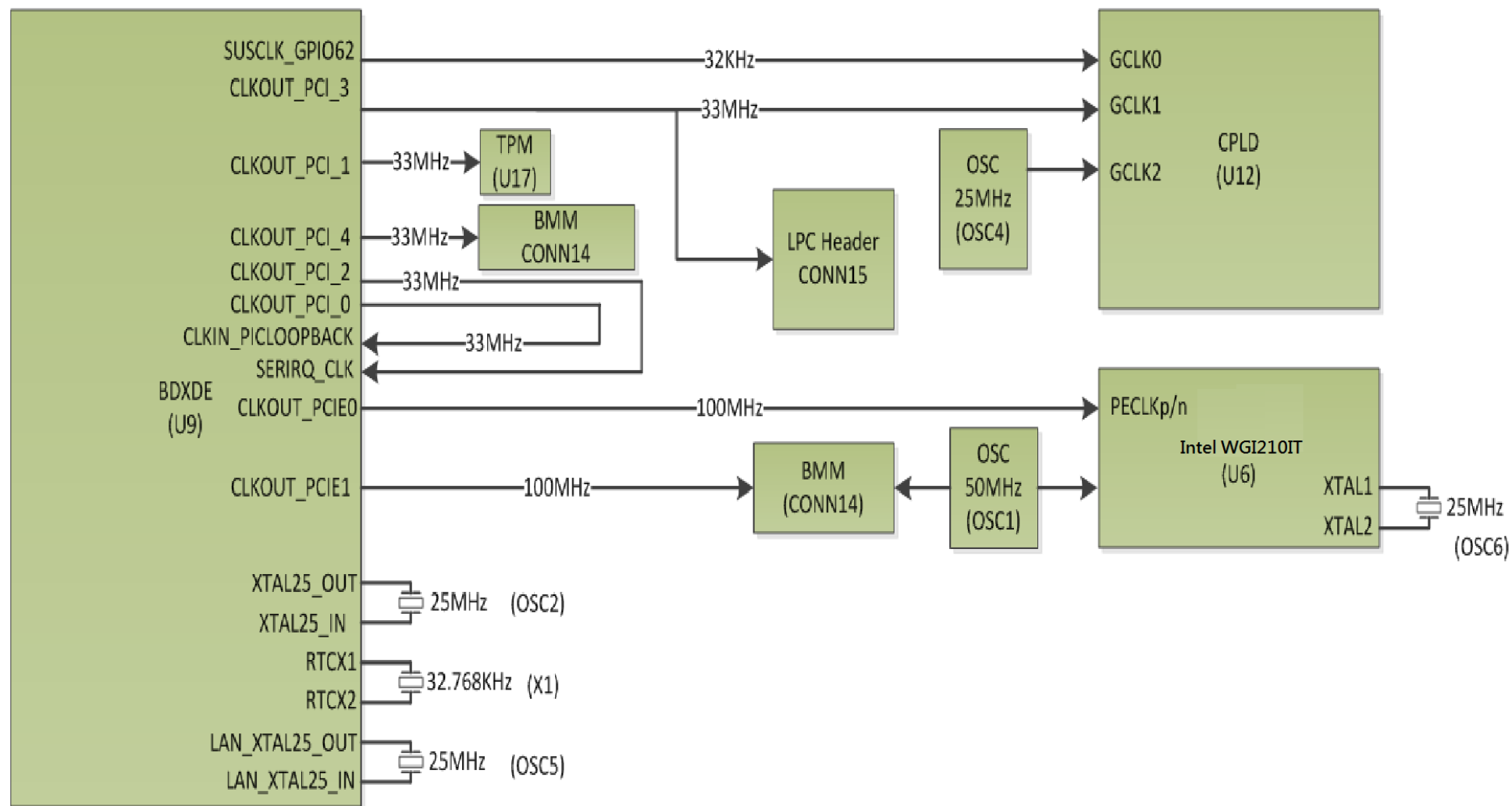
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Model Name		BDX-DE CPU Board	Rev	R0A
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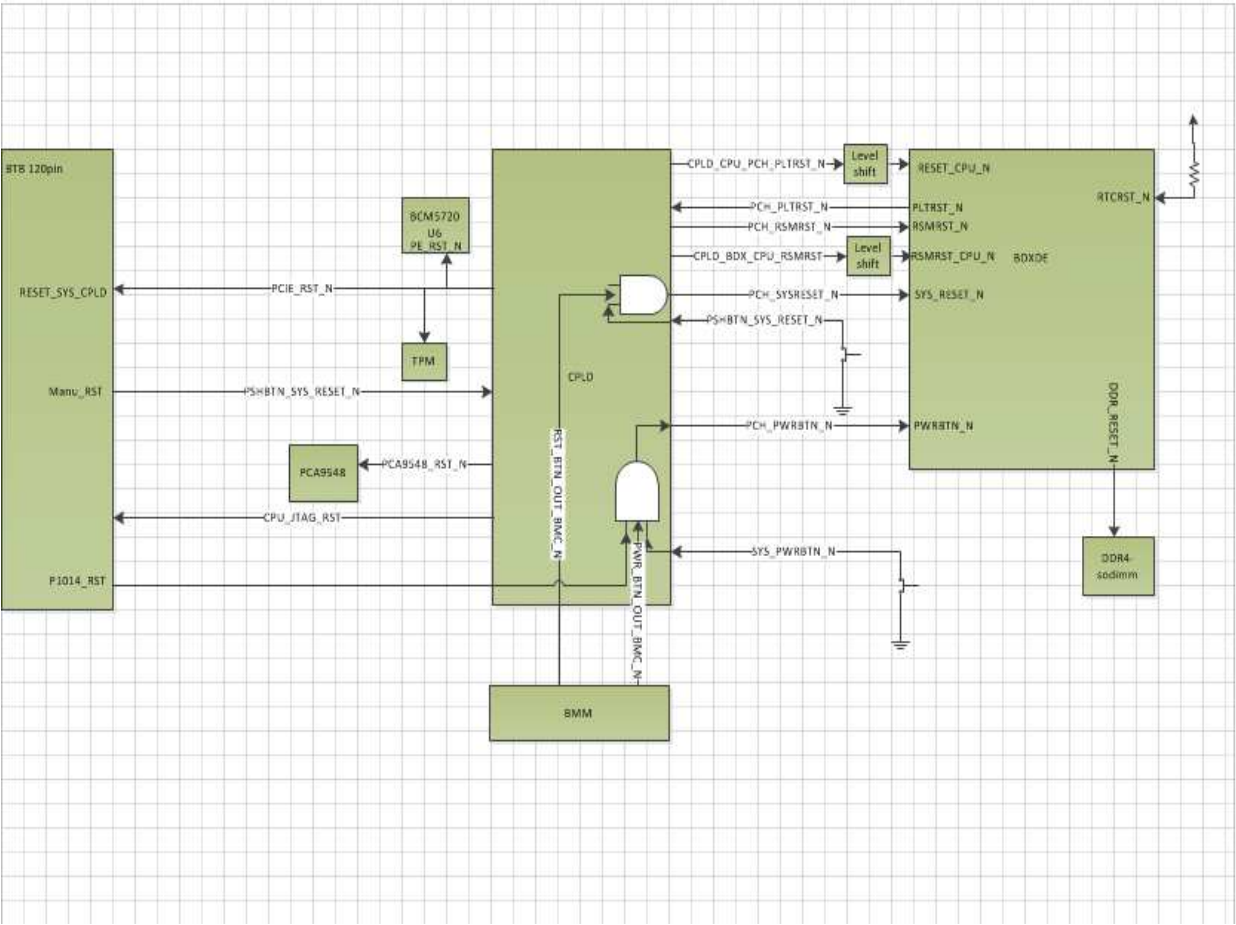
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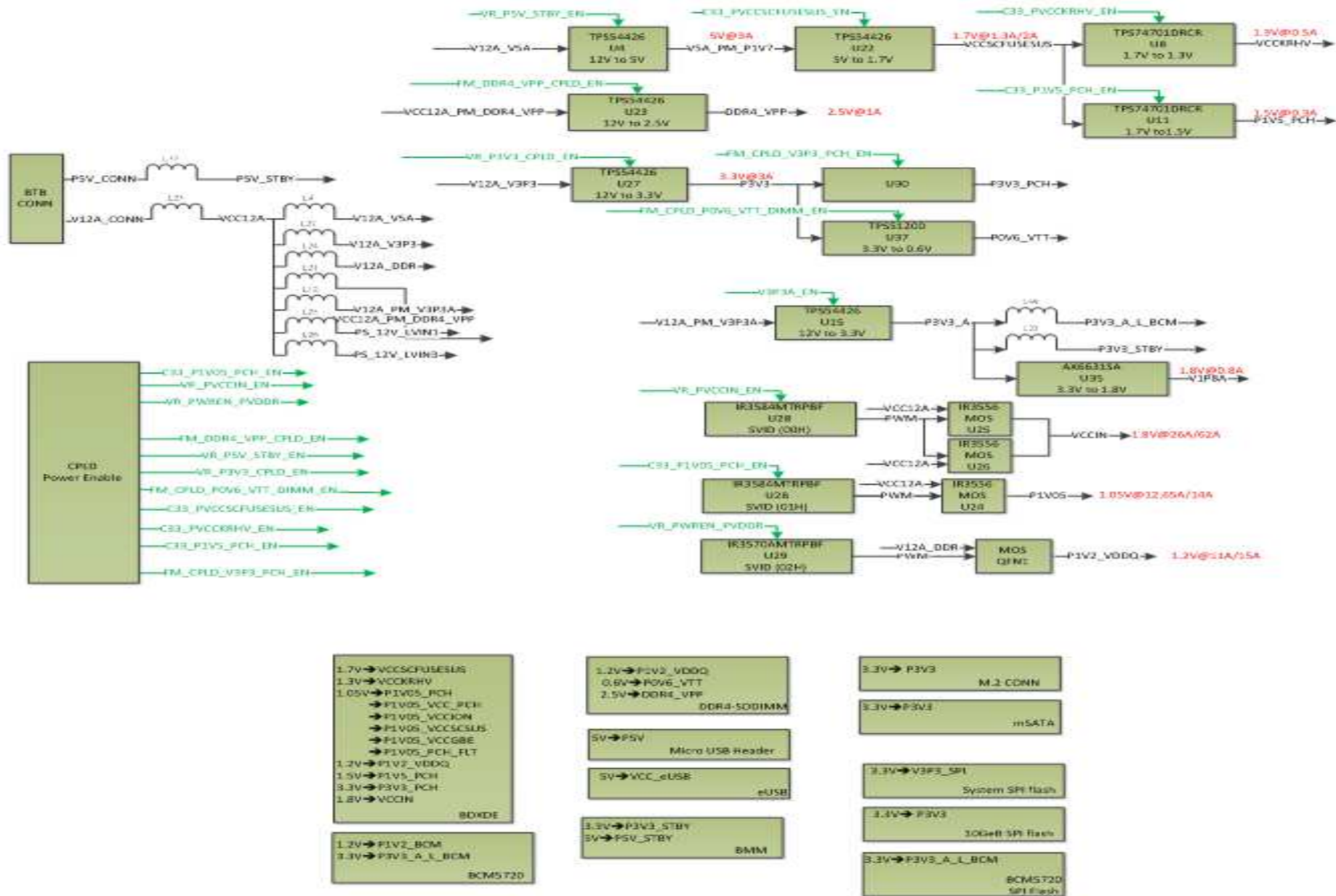
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Grangeville / TBC

CPLD

P3V3_A

CPLD checks 12V good

Standby rails

PSV_STBY

P3V3_STBY

10mS

Assert DPWROK

1mS

Assert APWROK

South Complex

VCCSCFUSESUS

VCCIOIN

VCCKRHV

VCCGBE

VCCSCSUS

10mS

Assert SC_PWRGD

10uS

Assert CPU_RSMRST

SLP_54 transitions high

Memory

DDR4_VPP

P1V2_VDDQ

Camelback Mountain

CPLD

P3V3_A

CPLD Checks 12V good

Standby rails

PSV_STBY

P3V3 (only standby rails come up)

10mS

Assert DPWROK

1mS

Assert APWROK

South Complex

VCCSCFUSESUS

P1V05

VCCKRHV

—Connected to P1V05

—Connected to P1V05

10mS

Assert SC_PWRGD

10uS

Assert CPU_RSMRST

Camelback Mountain does not monitor SLP sig.

Memory

DDR4_VPP

P1V2_VDDQ

P0V6_VTT_DIMM

PCH Core

P1V05_PROC_IO

P1V5_PCH

P3V3

CPU Core

VCCIN

Assert PCH_PWROK

1ms

Assert DRAM_PWROK

Assert SYS_PWRGD to PCH

PCH drives CPU_PWRGD_PCH to CPU

P0V6_VTT_DIMM

PCH Core

P1V05 comes up (ABOVE)

P1V5_PCH

PSV3_PCH – switched version of P3V3

CPU Core

VCCIN

Assert PCH_PWROK

1mS

Assert DRAM_PWROK

Assert SYS_PWRGD to PCH

PCH Drives CPU_PWRGD_PCH

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BroadWell_STRAP

SIGNAL	VALUE	Note
LOGSPARE4_DDR_STRAP	0	DDR3
	1	DDR4 (Default) ,IPU
PU_TXT_PLTEN	0	The platform is Intel TXT (Default) ,IPU to 1.05
	1	The platform is not Intel TXT
PU_TXT_AGENT	0	The socket is the Intel TXT Agent (default) ,IPD
	1	The socket is not the Intel TXT Agent
ADR_STATUS_CLR	0	Disable Intel ME Crypto Transport Layer Security cipher suite (with confidentiality)
	1	Enable Intel ME Crypto Transport Layer Security cipher suite (with confidentiality)
MANF_MODE_STRAP	0	Enable security measures defined in the Flash Descriptor (Default) ,IPD
	1	Disable Flash Descriptor Security
BDX_INTVRMEN	0	DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source
	1	Integrated VRMs enabled: DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.
	0	Disable PLL On-Die voltage regulator
CLK_M2_SUSCLK	1	Enable PLL On-Die voltage regulator (Default) ,IPU
	0	Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments.
PU_DSWODVREN	1	Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards. (Default)
	0	Disable No Reboot mode.
BDX_SPKR	1	Enable No Reboot mode (default , IPD)
	0 1	RESERVED
	1 0	RESERVED
	1 1	BOOT from SPI (default)
	0 0	BOOT from LPC
	0	SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS (default) ,IPD
	1	SoC TX is terminated to VCC/2.
	0	Build-in Self Test Disable (Default) ,IPU
	1	Build-in Self Test Enable
	0	Disable NVM Security (Default)
	1	Security Enabled
	0	SoC RX is terminated to VSS (default) ,IPD
	1	SoC RX is terminated to 1/2 VCC
	0	SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. (Default) ,IPU
	1	SoC is in DC-coupling mode.
	0	Enable Top Swap mode.
	1	Disable Top Swap mode. Default
		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
		This signal has a weak internal pull-up. This pin must not be driven low until after rising edge of RSMRST_N.
	0	Integrated Service Processor Boot Mode Disabled. (Default) ,IPD
	1	Integrated Service Processor Boot Mode Enable
	0	Safe Mode Boot Disabled (Default) ,IPD
	1	Safe Mode Boot Enabled
	0	Debug Mode
	1	Normal Mode
	0	CLJD0
	0	CLJD1
	0	CLJD2
	0	is pin should have a 5.1K ohm pull down to GND. There is weak internal pull down.
	0	is pin should have a 5.1K ohm pull down to GND. There is weak internal pull down.
	0	is pin should have a 5.1K ohm pull down to GND. There is weak internal pull down.
	0	is pin should have a 5.1K ohm pull down to GND. There is weak internal pull down.
	1	Recommend 5.1k ohm pull up to VCCIOIN. There is no internal pull up or pull down.
	0	Recommend 5.1k ohm pull down to GND. There is no internal pull up or pull down.
	0	Disable NVM Security (Default)
	1	Security Enabled
	0	Recommend 5.1K ohm pull up to VCCIOIN. There is no internal pull up or pull down.
	0	LAN available in S5 for Wol.
	1	LAN not available in S5. Manageability is disabled. (Default)

BroadWell_STRAP

SIGNAL	VALUE	Note
(RP_LAN_MDIO_DIR_CTL0_0,	0,0	Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1.
	0,1	Port 1 is disabled. Port 0 is enabled.
	1,0	Reserved
	1,1	Both Port 0 and 1 are enabled. (Default)
	0	Separate SVID controllers.
	1	VCC3CSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply (default)

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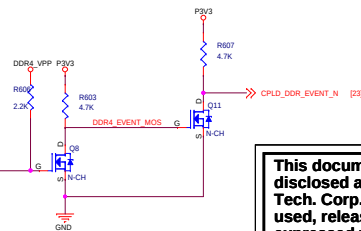
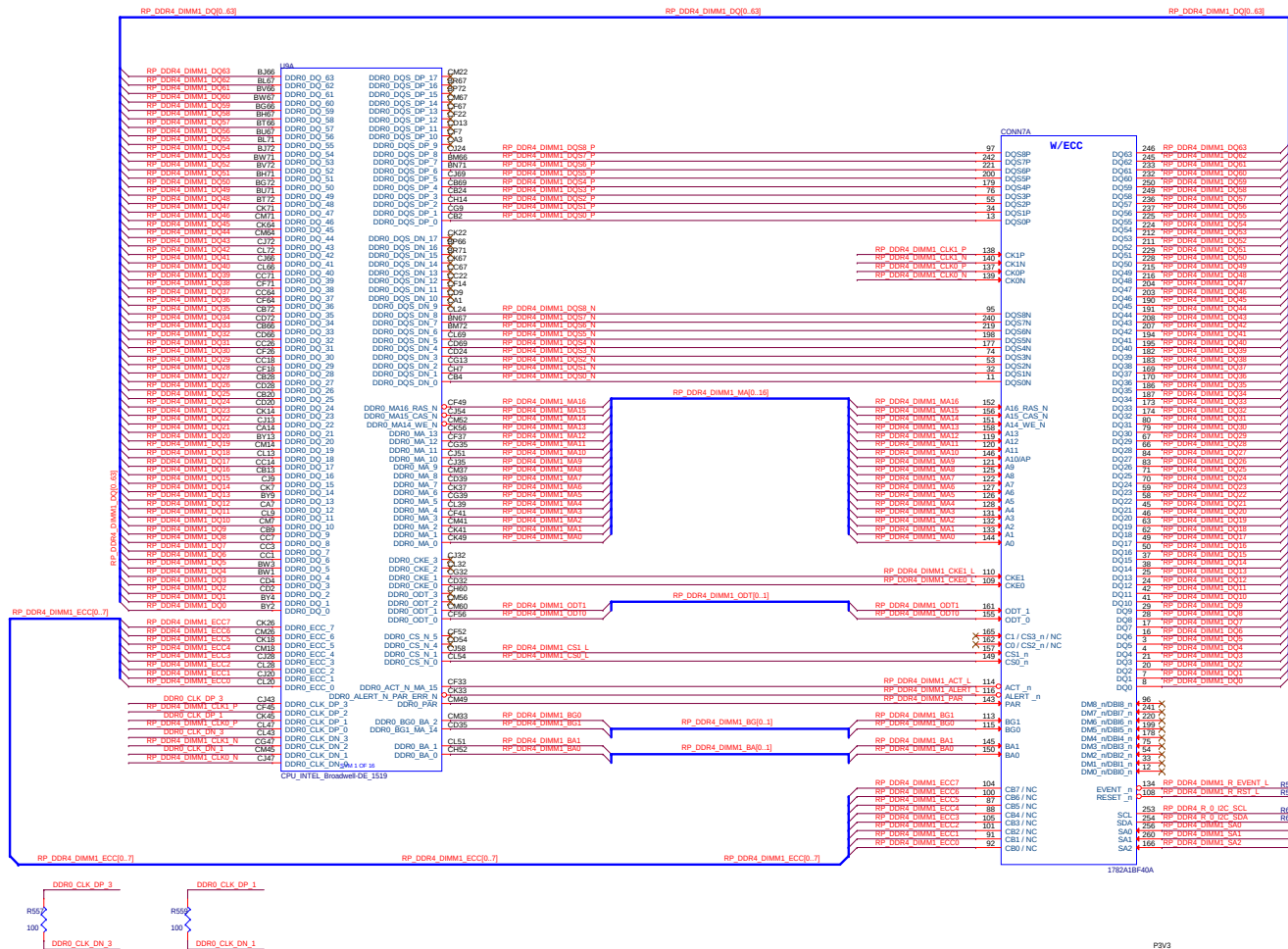
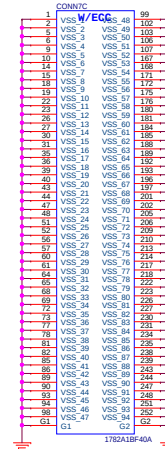
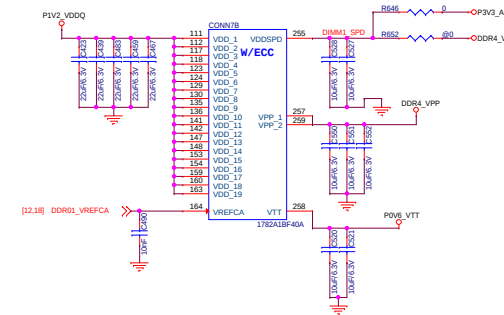
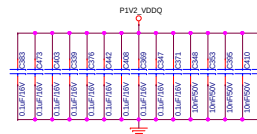
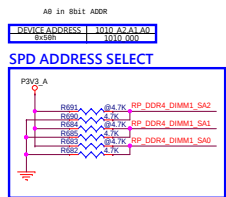
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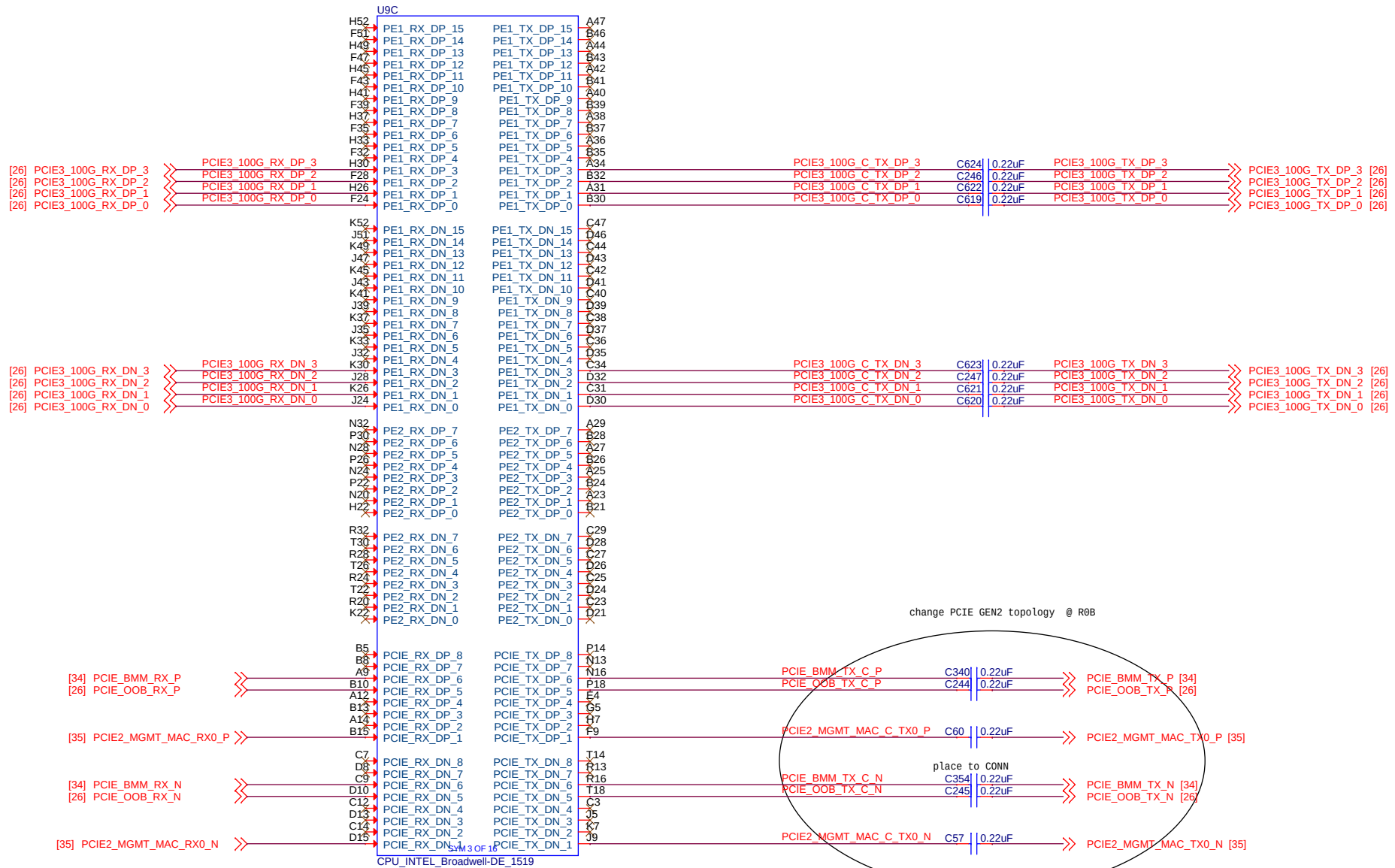
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Supply voltage	Input	Input/output	
$V_{CC} = V_{CC1}$	CNC	A	B
0.8 V to 3.6 V	L	A = B	input
0.8 V to 3.6 V	H	input	B = A
CNC	X	Z	Z

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FMA - HW01008 - 01 R01



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CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

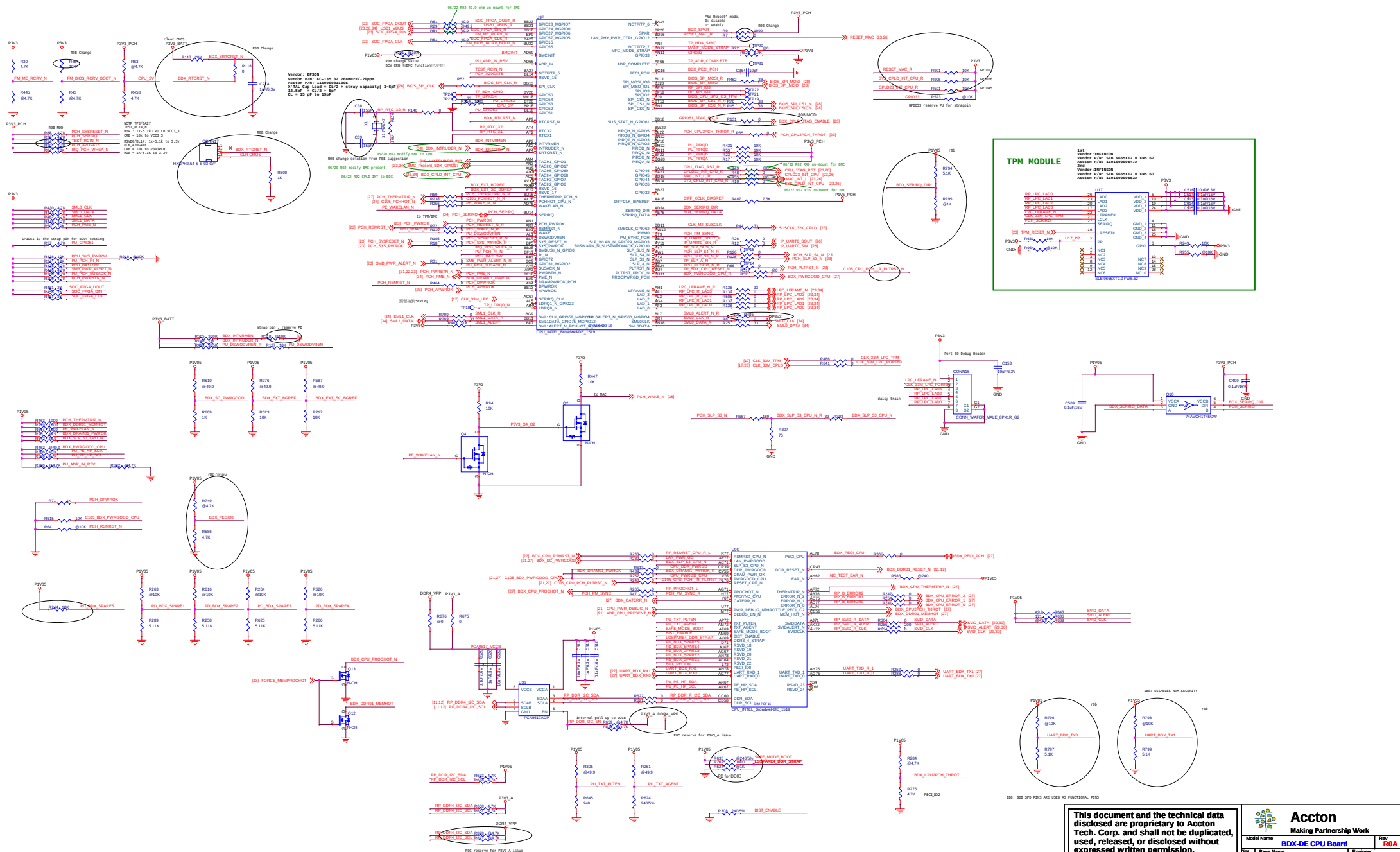
CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

Supply voltage	Input	Input/output ⁽²⁾	
V _{CC(A)} = V _{CC(B)}	DIR ⁽¹⁾	A	B
0.8 V to 3.6 V	L	A = B	input
0.8 V to 3.6 V	H	input	B = A
GND ⁽³⁾	X	Z	Z



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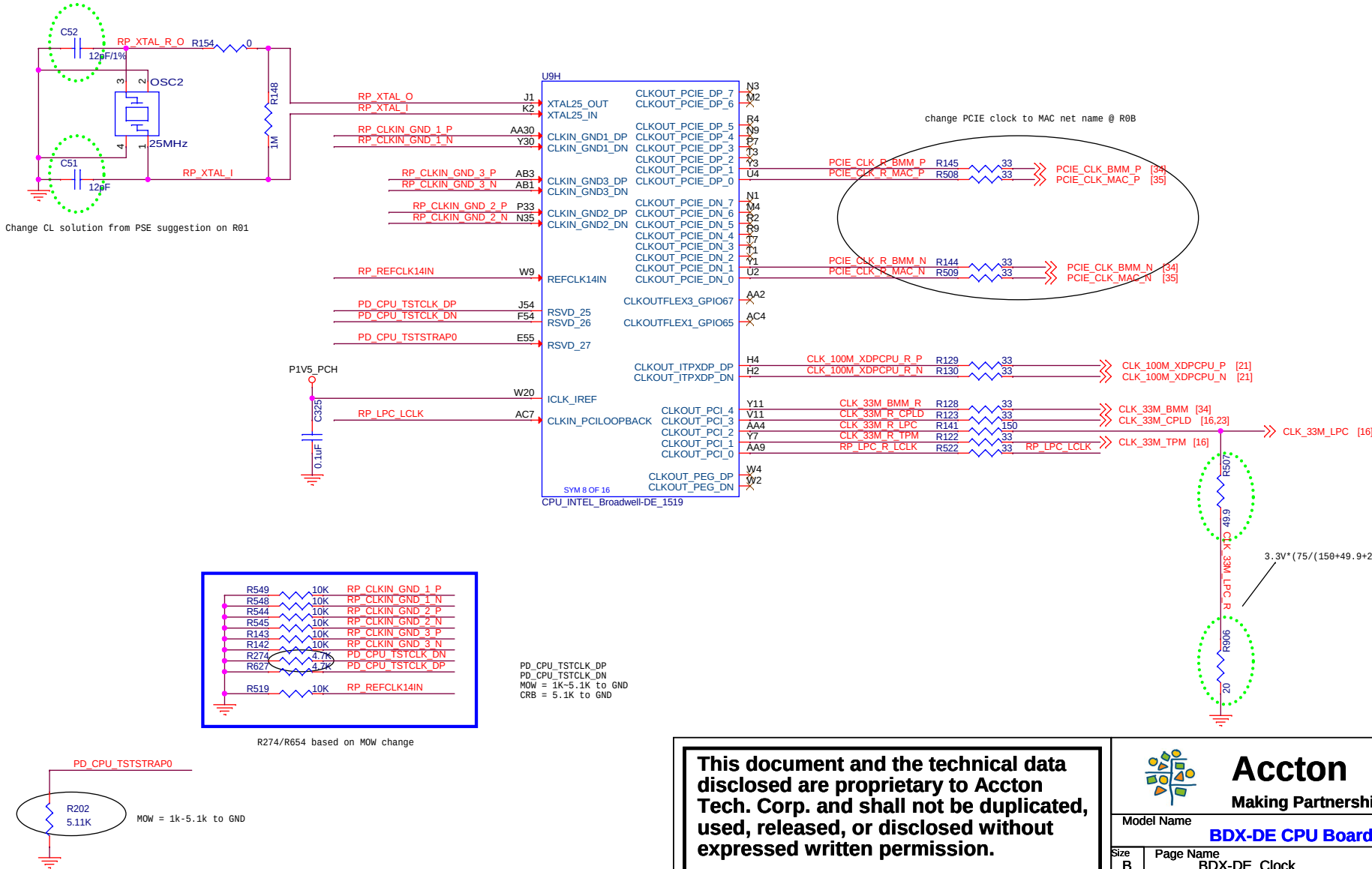
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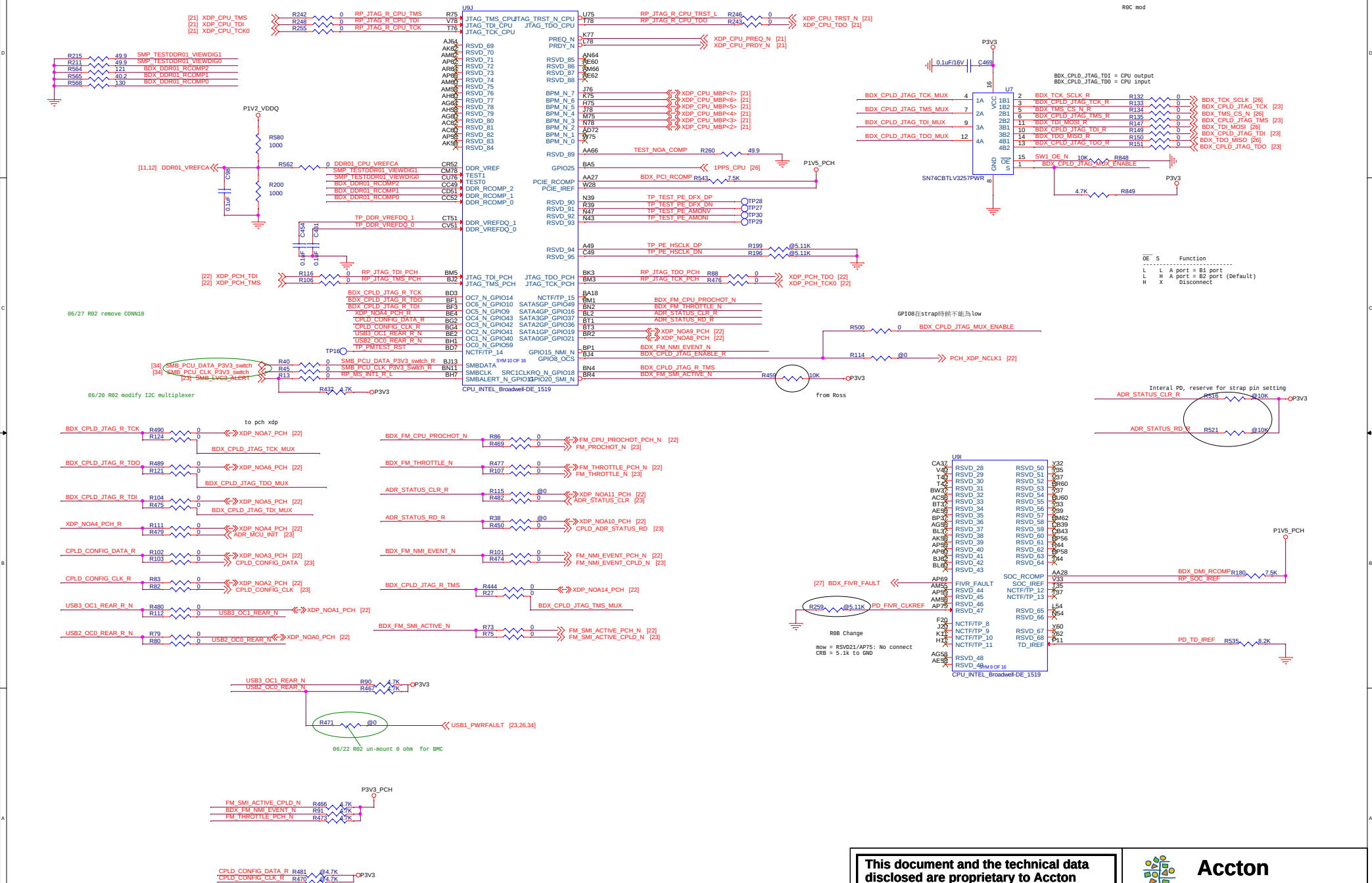
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Model Name BDX-DE CPU Board		Rev ROA
Site D	Project Name BDX-DE_SYSTEM&TPM	Engineer Dino_Lin
Date Mar 21, 2018	By lpsell	18 - 01 - 35

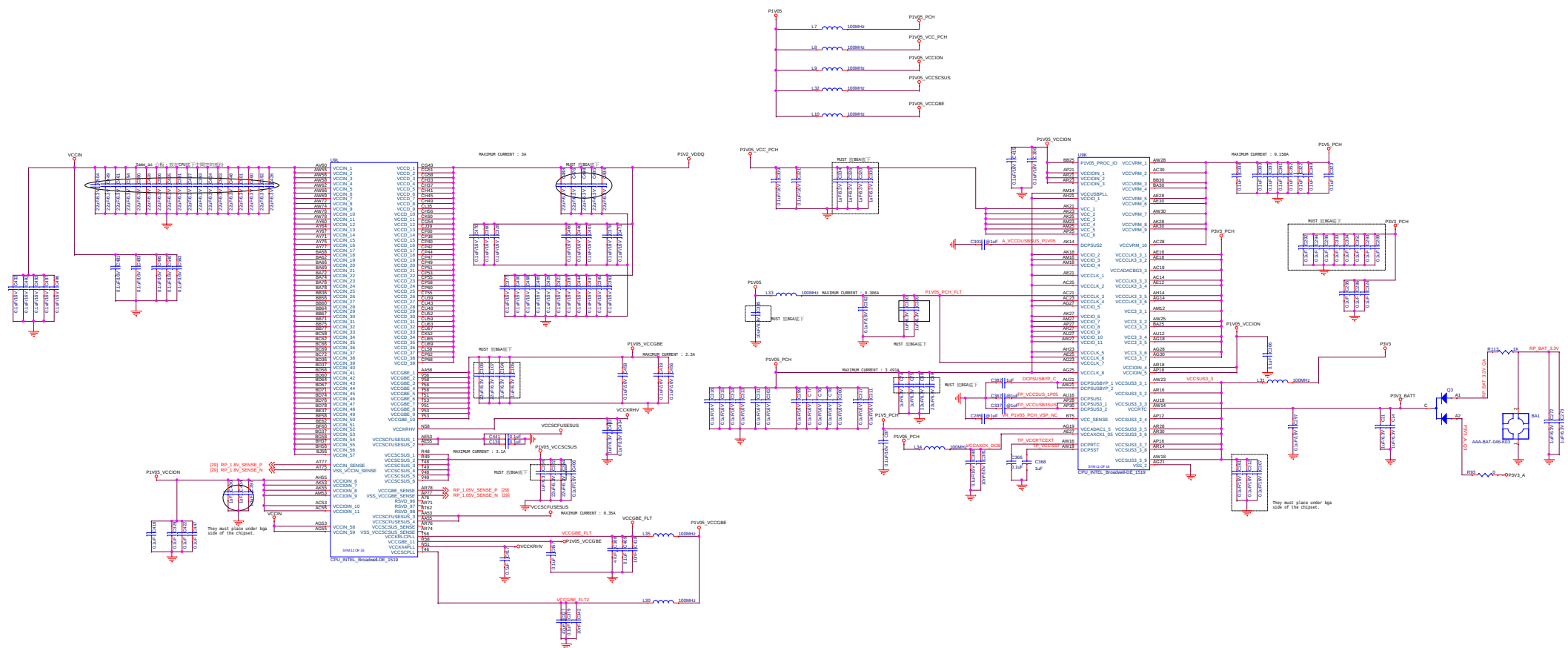
FMA-HW01008-01 R01

Vendor: PSE
Vendor P/N: FL2500096 25MHz+/-15ppm
Accton P/N: 116000000058A
X'TAL Cap Load = CL/2 + stray-capacity(3-5pF)
12pF = CL/2 + (3pF to 5pF)
CL = 14pF to 18pF





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HSB1

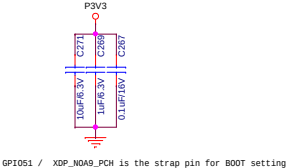
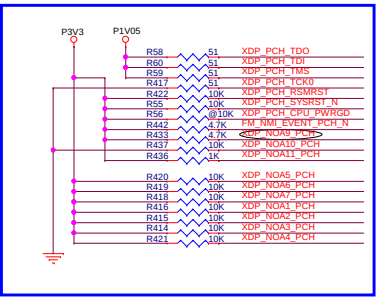
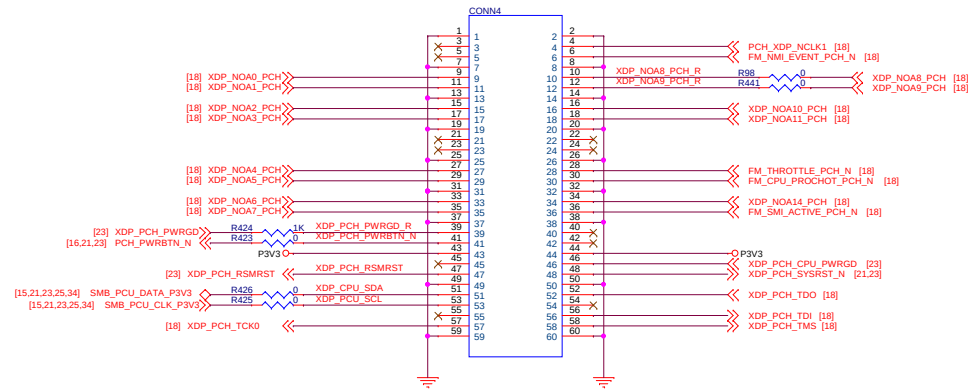
NC1	NC1
NC2	NC2
NC3	NC3
NC4	NC4

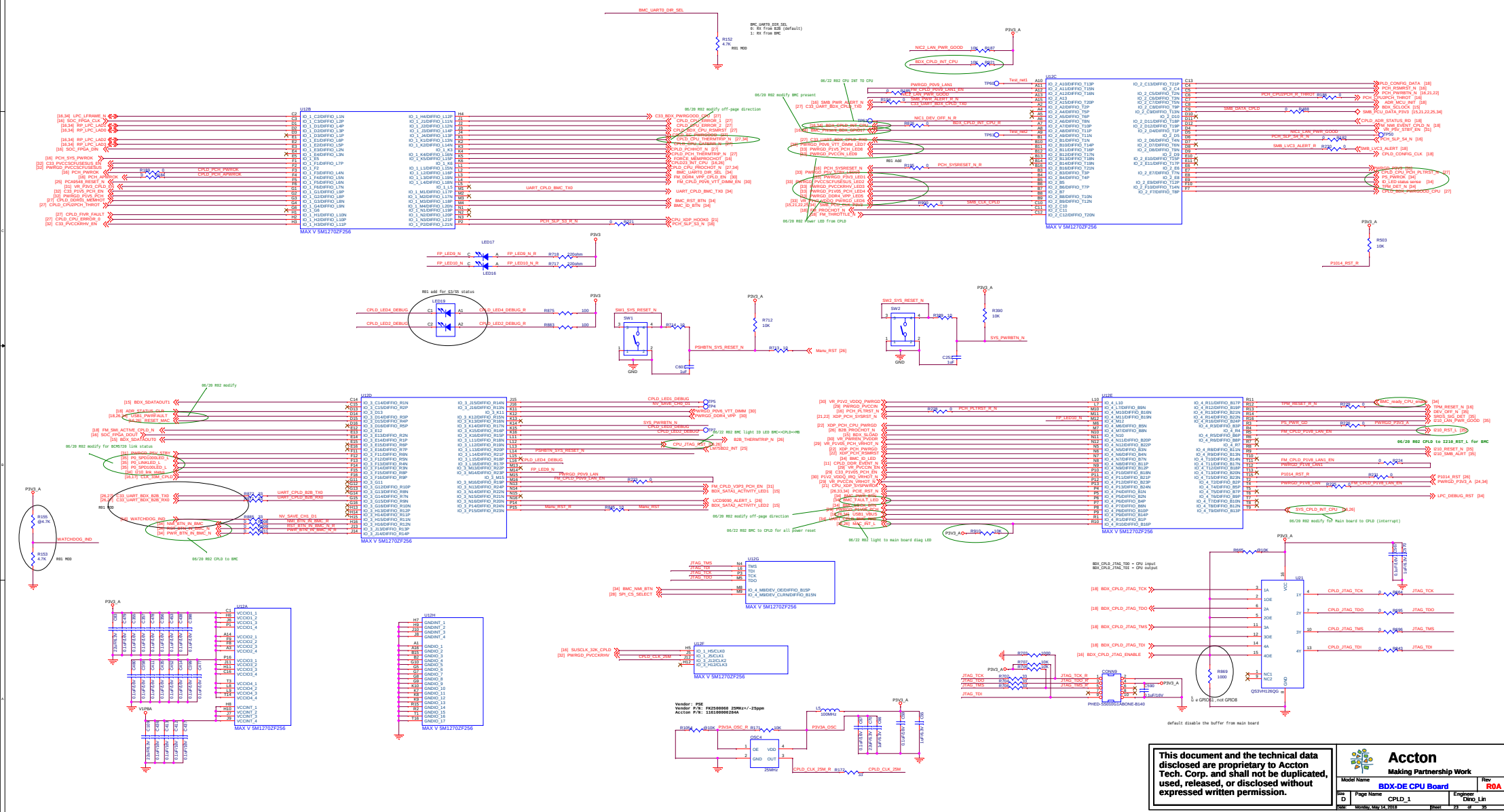
Heatsink Bracket

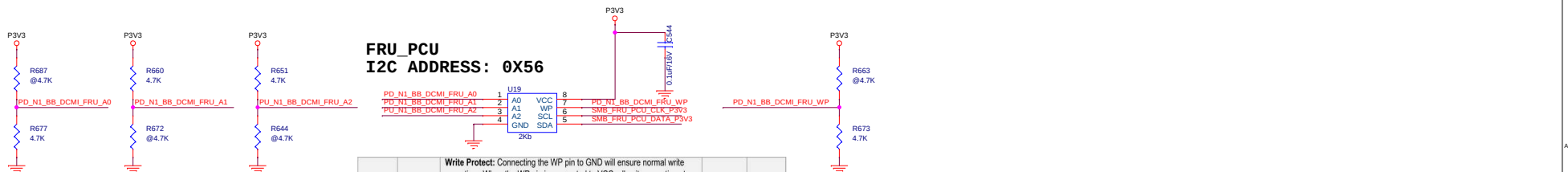
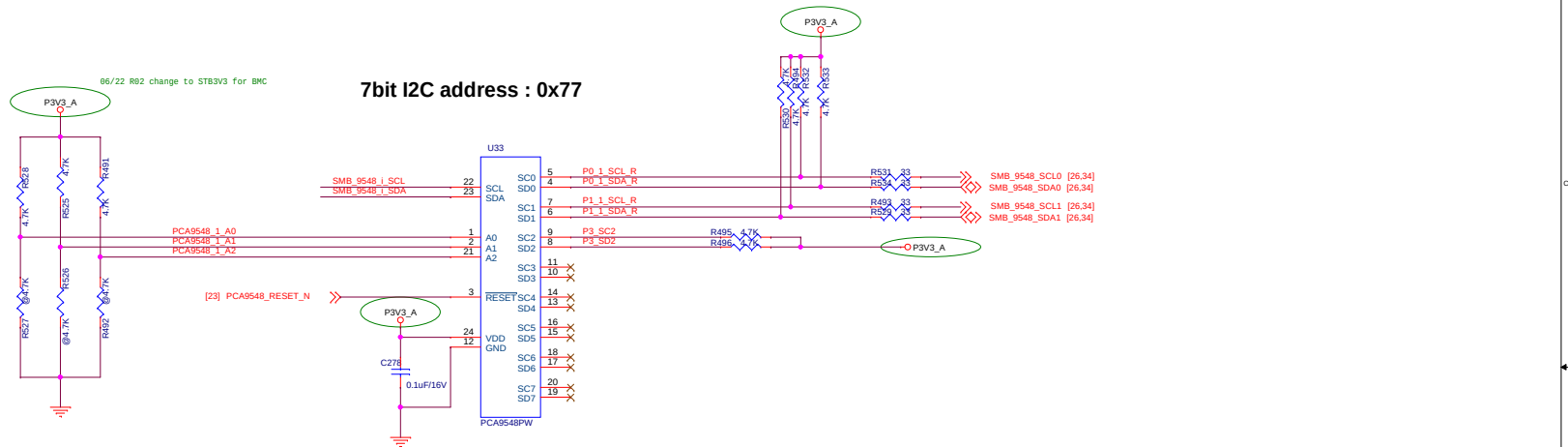


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7	WP	Write Protect: Connecting the WP pin to GND will ensure normal write operations. When the WP pin is connected to VCC, all write operations to the memory are inhibited. Refer to Note 1 for behavior of the pin when not connected.	High	Input		This document and the technical data  Aspen
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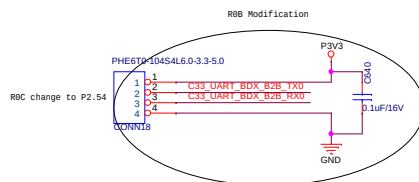
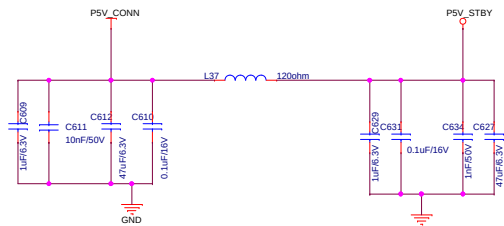
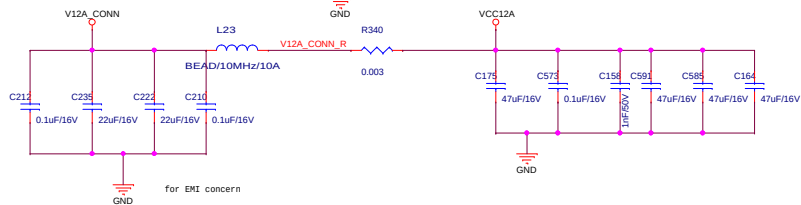
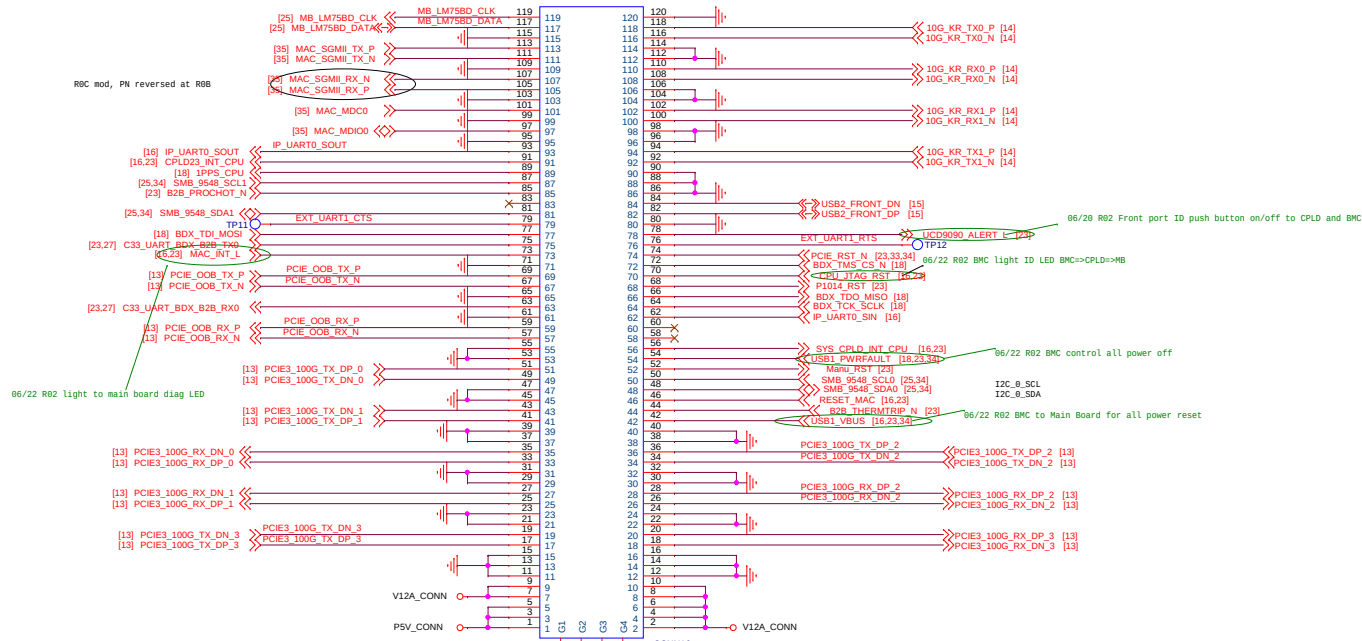


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footprint 改@connm_d5x5d32_2x8@sp_combo_1

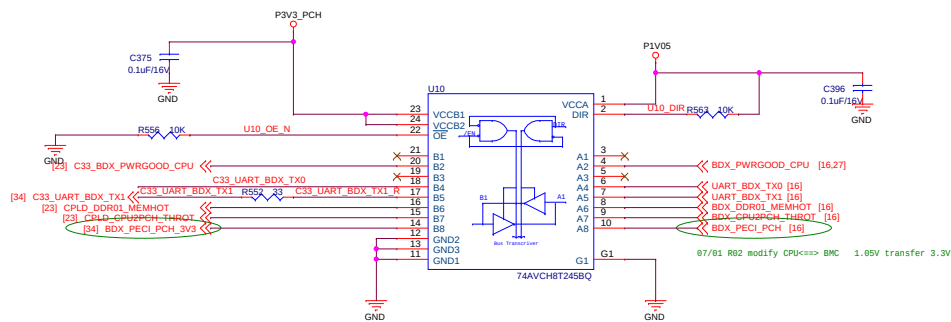
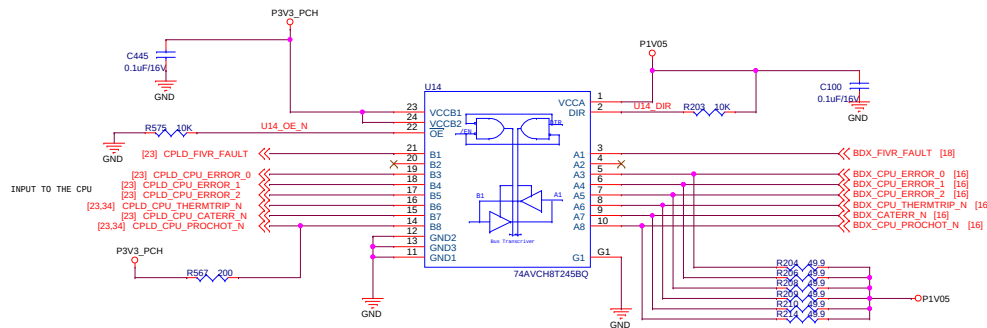
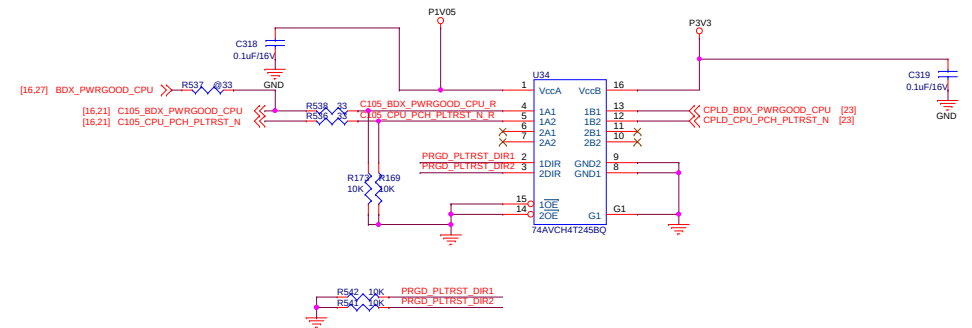
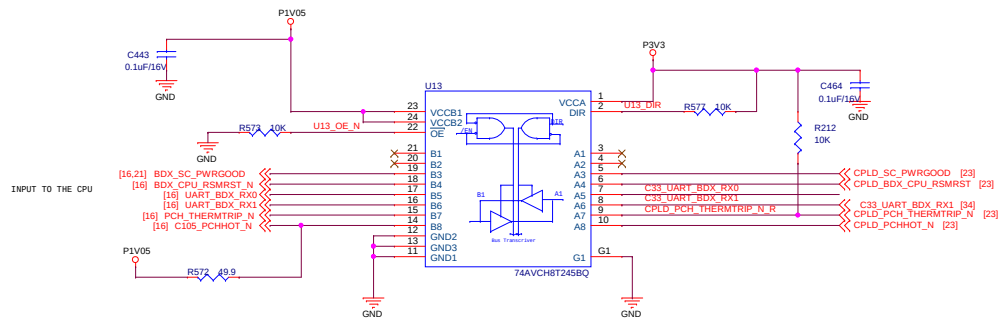


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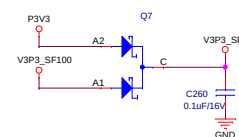


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Size	Page Name	Engineer
C	Level Shifter	Dino_Lin
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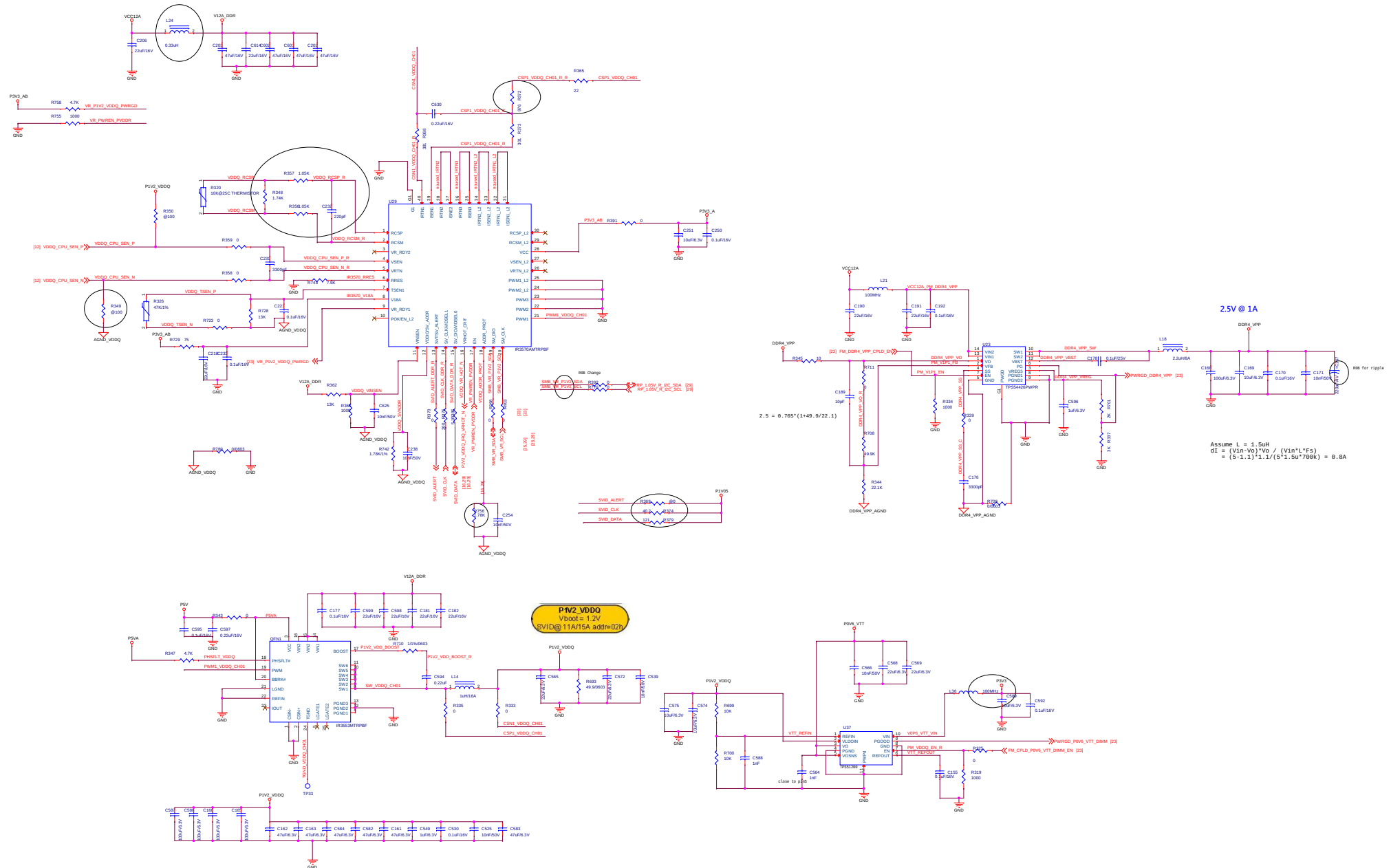




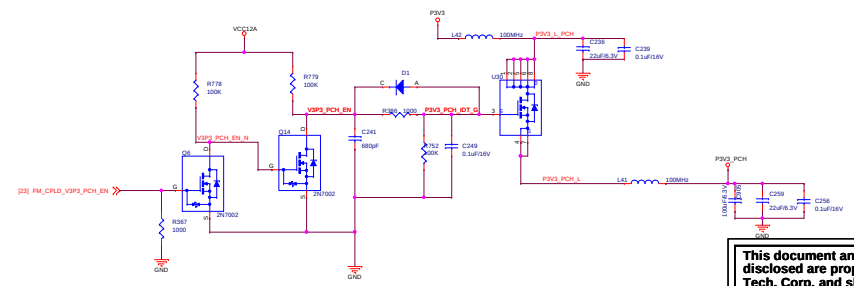
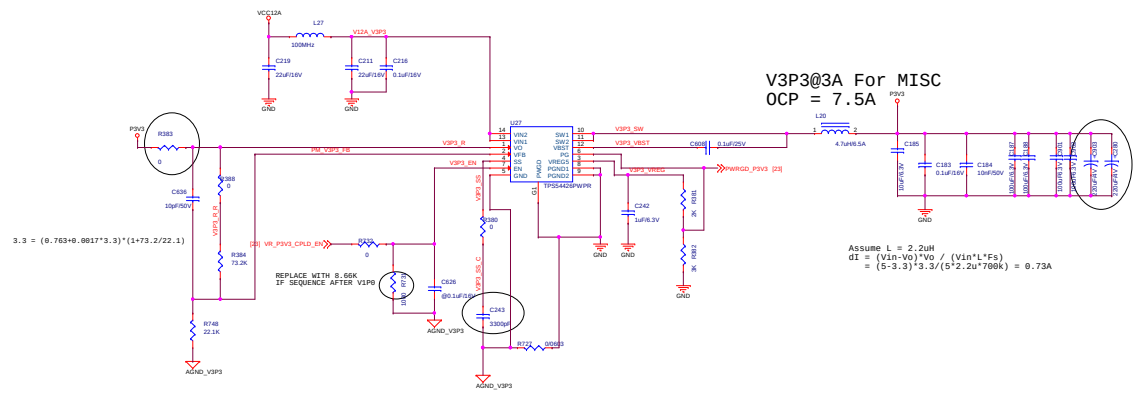
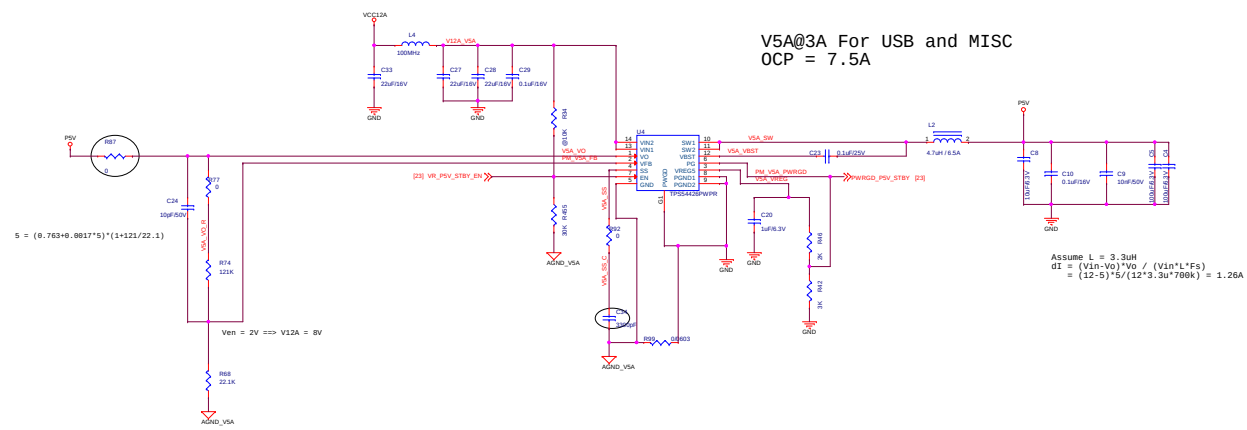
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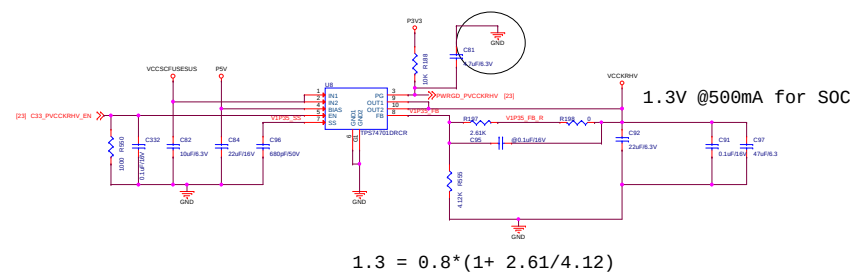
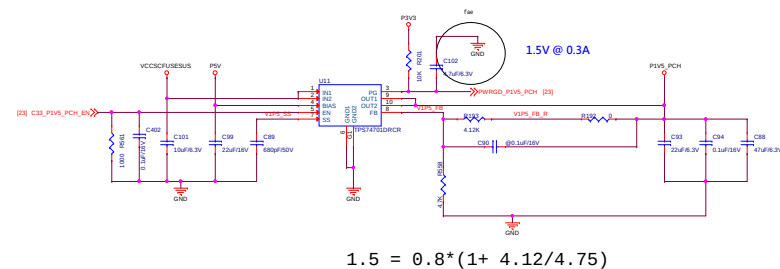
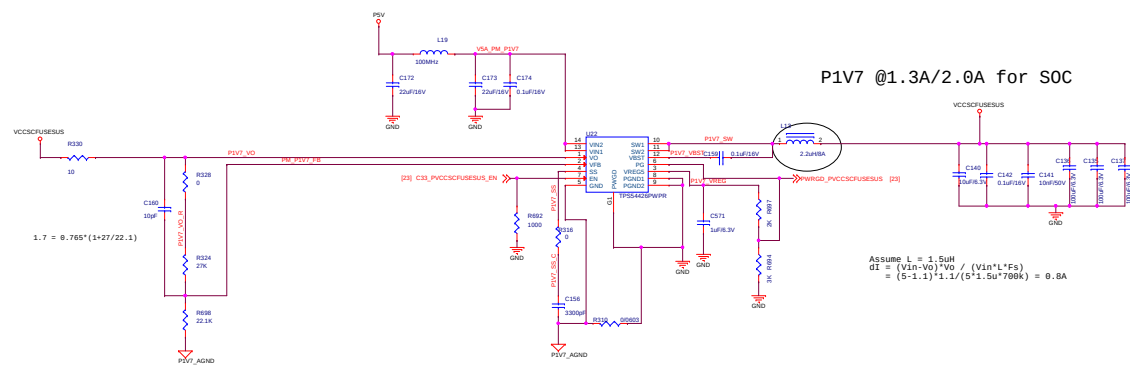
Model Name	BXD-DE CPU Board	Rev R0A
Page Name	SPI	Engineer <u>Dino_Lin</u>
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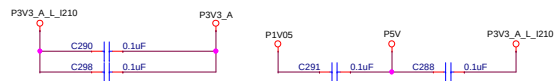
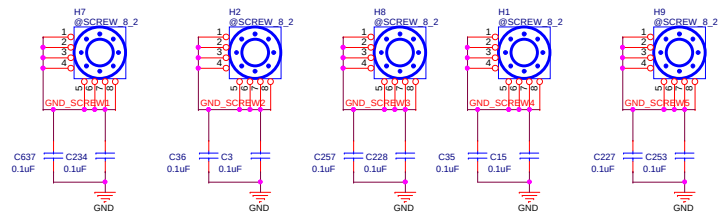
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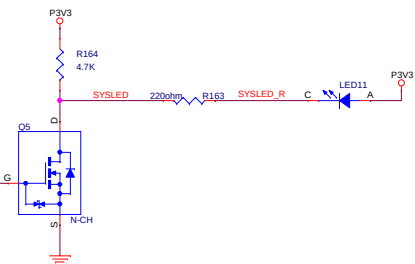
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[23,26,34] PCIE_RST_N



Sequence

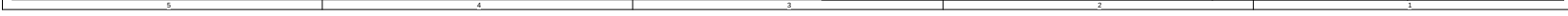
1. P3V3_A
2. P5V
3. P3V3
4. P1V7
5. P1V3
6. P1V05
7. VPP
8. VDDQ
9. VTT / VCCIN / P1V5 /

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